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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/506,502	02/17/2000	Albert Ren-Rui Wang	83818/0261848	6419

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EXAMINER	
DO, THUAN V	
ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 06/13/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application No. 09/506,502	Applicant(s) WANG ET AL.	
	Examiner Thuan Do	Art Unit 2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Peri d f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-49* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-46,48,49* is/are rejected.

7)☒ Claim(s) *47* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 February 2000* is/are: a)☐ accepted or b)☒ objected to by the ~~Examiner~~ draftperson.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Pri rity under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4,5* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

1. Claims 1-49 are pending in this office action.

Claims

Claim 1, the term "...a predetermined portion and a user-defined portion ..." ,

claim 32, the term "...a software data type not found..."

claim 48, the term "...a processor instruction raises the exception..."

Clarification or correction is required.

Specification

Page 1, line 10 the "attorney docket number 83818/261871" should be replaced by an application serial number of Patent Office. Correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (e) the invention was described in-
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

2. Claims 1-46,48,49 are rejected under 35 U.S.C. 102(e) as being unpatentable over Killian et al., Pat. No. 6,477,697.

Regarding claim 1: Killian teaches a system comprising:

hardware generation means for, based on a configuration specification including a predetermined portion and a user-defined portion (Figure 6, with a diagram of

additional logic), generating a description of a hardware implementation of the processor (col. 2, lines 40-47) ; and

software generation means for, based on the configuration specification, generating software development tools specific to the hardware implementation (col. 2, lines 40-47 with new instructions in a software tool);

wherein the hardware generation means is for, based on the user-defined portion of the configuration specification(Figure 6, with a diagram of additional logic), including a user-defined register file (col. 4, lines 1-11) in the description of the hardware implementation of the processor (col. 2, lines 40-47); and

the software generation means is for, based on the user-defined portion, including software related to the user-defined processor register file (col. 4, lines 1-11) in the software development tools (col. 2, line 58 through col. 3, line 5) .

Regarding claim 2: Killian teaches a system with accessing elements (col. 7, lines 16-20).

Regarding claim 3: Killian teaches a system with the description of the hardware implementation (col. 2, lines 58-67).

Regarding claims 4,5: Killian teaches a system with the register file (col. 4, lines 1-11).

Regarding claim 6: Killian teaches a system with ports (col. 3, lines 42-57).

Regarding claims 7,16: Killian teaches a system with scheduling information (col. 14, lines 28-38).

Regarding claim 8: Killian teaches a system with minimize data staging costs (col. 1, lines 38-48).

Regarding claim 9: Killian teaches a system with pipeline logic (figure 4).

Regarding claims 10-12: Killian teaches a system with operands (col. 4, lines 23-27).

Regarding claim 13: Killian teaches a system with bypass logic (col. 10, lines 46-60).

Regarding claims 14,15: Killian teaches a system with interlock logics (col. 17, lines 6-15).

Regarding claim 17: Killian teaches a system with instruction operand and state usage descriptions (col. 4, lines 23-27 and col. 1, lines 30-35).

Regarding claims 18-22,28,29,33,35-38: These claims teach a system for the same system of claim 1 and rejected in the same rationale.

Regarding claim 23: Killian teaches a system with conditionally writes (col. 4, lines 1-11).

Regarding claim 24: Killian teaches a system with diagnostic tests (col. 3, lines 42-58).

Regarding claim 25: Killian teaches a system with:

both reference and implementation semantics (col. 2, lines 41-47).

verify design correctness (col. 15, lines 33-43).

Regarding claims 26,27: Killian teaches a system with instruction and diagnostics test (col. 3, lines 42-58).

Regarding claim 30: Killian teaches a system with restore sequences (col. 7, lines 41-67).

Regarding claim 31: Killian teaches a system with saving less than an entirety of processor state (col. 8, lines 38-50).

Regarding claim 32: Killian teaches a system with a software data type not found (col. 2, lines 12-25 using "...extended to enhance the functionality of the processor and customize..." to select the not found function in the software).

Regarding claim 34: Killian teaches a system with generating a compiler and allocating program variables (col. 7, lines 41-52).

Regarding claim 39: Killian teaches a system comprising:

hardware generation means for, based on a configuration specification including a predetermined portion and a user-defined portion, generating a description of a hardware implementation of the processor (Figure 6 and col. 2, lines 40-47) ; and

software generation means for, based on the configuration specification, generating software development tools specific to the hardware implementation (col. 2, lines 40-47 with new instructions in a software tool);

wherein the configuration specification includes a statement specifying scheduling information of instructions used in the software development tools (col. 2, lines 40-47);

the hardware generation means is for, based on the configuration specification, generating a description of at least one of pipeline logic, pipeline stalling logic (figure 4 with pipeline structure) and instruction rescheduling logic (col. 14, lines 28-39 using scheduling algorithm with RUR restoring state function).

Regarding claim 40: Killian teaches a system with an operand of an instruction enters a pipeline (col. 4, lines 23-27).

Regarding claim 41: Killian teaches a system with an instruction exits a pipeline (figure 4).

Regarding claim 42: Killian teaches a system with the software generation and the scheduling information (col. 2, lines 40-47 and col. 14, lines 28-38).

Regarding claim 43: Killian teaches a system with processor cycles (col. 1, lines 23-36).

Regarding claim 44: Killian teaches a system with the independent of a target pipeline and a pipeline description separate from the instruction (col. 10, lines 28-45 using new instructions).

Regarding claims 45,46: This claim teaches a system similar to the system of claim 1 and rejected in the same rationale.

Regarding claim 48: Killian teaches a system comprising:

hardware generation means for, based on a configuration specification including a predetermined portion and a user-defined portion, generating a description of a hardware implementation of the processor (Figure 6 and col. 2, lines 40-47); and

software generation means for, based on the configuration specification, generating software development tools specific to the hardware implementation (col. 2, lines 40-47 with new instructions in a software tool) ;

wherein the configuration specification includes a specification of a processor exception and when a processor instruction raises the exception (col. 10, lines 62-67); and

the hardware generation is for generating hardware supporting that exception (col. 10, lines 62-67) as part of the processor hardware implementation (Figure 6 and col. 2, lines 40-47).

Regarding claim 49: Killian teaches a system comprising:

hardware simulation (col. 2, lines 58-67 using a simulator) means for executing a hardware description of an extensible processor (figure 2, box 96);

software simulation means for executing a software: reference model of the extensible processor; and

cosimulation means for operating the hardware simulation means and the software simulation means and comparing results of simulations therefrom to establish correspondence between the hardware description of the extensible processor and the software reference model of the extensible processor (col. 13, lines 56-64 teaches "compared with various constants to form various selection signals which are used to select certain bits from the state registers" that means comparing various register states for cosimulation function) .

Allowable Subject Matter

3. Claim 47 is objected to as being dependent upon a rejected base claims, but would be allowable if rewritten in independent form including all of the limitations of the base claims and any intervening claims. The reason for allowance is that the prior art of record does not teach the details of the dependant claim.

CONTACT INFORMATION

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thuan Do whose telephone number is 703-305-2362. The examiner can normally be reached on Monday-Friday 8:30-5:30 (except 2nd Fridays).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 703-308-1323. The fax phone numbers for the organization where this application or proceeding is assigned are

703305-3431 for regular communications and 703-305-3431 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0596.

Thuan Do
Patent examiner
6/10/03